Amendments to the Claims

1. (original) A phase-locked loop system that provides a loop output signal in response to a reference signal, comprising:

an oscillator network that generates said loop output signal with a frequency that varies in response to a control voltage and to a frequency-determining parameter;

a feedback loop that generates said control voltage in response to the phase difference between said reference signal and a loop feedback signal wherein said feedback loop includes a loop frequency divider that has a divisor N and generates said loop feedback signal in response to said loop output signal; and

a controller that increments said frequency-determining parameter to maintain said control voltage within a predetermined control-voltage range.

2. (original) The system of claim 1, wherein said controller is configured to monitor said control voltage and increment said frequency-determining parameter each time said control voltage reaches a limit of said control-voltage range.

3. (original) The system of claim 1, wherein said oscillator network includes:

an oscillator that generates an oscillator signal; and

an output frequency divider that has a frequency divisor X and that provides said loop output signal in response to said oscillator signal;

and wherein said frequency divisor X is responsive to said controller so that said frequency-determining parameter is said frequency divisor X.

4. (original) The system of claim 3, wherein said controller is configured to monitor said control voltage and increment said frequency divisor X each time said control voltage reaches a limit of said control-voltage range.

5. (original) The system of claim 1, wherein said controller includes a comparator that compares said control voltage to said control-voltage range.

6. (currently amended) The system of claim 1, wherein said feedback loop includes ~~incudes~~:

a phase detector that generates an error signal in response to the phase difference between said ~~said~~ reference signal and said loop feedback signal;

a charge pump that provides drive currents in response to said error signal; and

a loop filter that generates said control voltage in response to said drive currents.

7. (original) A phase-locked loop system that provides a loop output signal in response to a reference signal, comprising:

an oscillator that generates said loop output signal with a frequency that varies in response to a control voltage and to a frequency-determining parameter;

a feedback loop that generates said control voltage in response to the phase difference between said reference signal and a loop feedback signal wherein said feedback loop includes a loop frequency divider that has a divisor N and generates said loop feedback signal in response to said loop output signal; and

a controller that increments said frequency-determining parameter to maintain said control voltage within a predetermined control-voltage range.

8. (original) The system of claim 7, wherein said controller is configured to monitor said control voltage and increment said frequency-determining parameter each time said control voltage reaches a limit of said control-voltage range.

9. (original) The system of claim 7, wherein said oscillator includes:

a plurality of inverters; and

a plurality of switches that each couple a different number of said inverters in a ring in response to said controller;

said frequency-determining parameter thereby formed by said inverters.

10. (original) The system of claim 9, wherein said controller is configured to monitor said control voltage and command at least one of said switches each time said control voltage reaches a limit of said control-voltage range.

11. (original) The system of claim 7, wherein said oscillator includes a ring of inverters that each have a plurality of resistive loads which can be selected by said controller, said frequency-determining parameter thereby formed by said resistive loads.

12. (original) The system of claim 11, wherein said controller is configured to monitor said control voltage and select at least one of said resistive loads each time said control voltage reaches a limit of said control-voltage range.

13. (original) The system of claim 7, wherein said oscillator includes a ring of inverters that each have a plurality of capacitive loads which can be selected by said controller, said frequency-determining parameter thereby formed by said capacitive loads.

14. (original) The system of claim 13, wherein said controller is configured to monitor said control voltage and select at least one of said capacitive loads each time said control voltage reaches a limit of said control-voltage range.

15. (original) The system of claim 7, wherein said oscillator includes a ring of inverters that each have a plurality of current sources which can be selected by said controller, said frequency-determining parameter thereby formed by said current sources.

16. (original) The system of claim 15, wherein said controller is configured to monitor said control voltage and select at least one of said current sources each time said control voltage reaches a limit of said control-voltage range.

17. (currently amended) The system of claim 16, wherein said controller includes a comparator that compares said control voltage to said control-voltage range ~~oscillator includes a ring of inverters~~.

18. (original) The system of claim 7, wherein said oscillator includes a ring of inverters that each includes:

a voltage-to-current converter that provides a tail current in response to said control voltage;

a pair of loads; and

a differential pair of transistors that steer said tail current between said loads in response to a signal from another of said inverters.

19. (original) The system of claim 18, wherein said loads include parallel resistive and capacitive loads.

20. (currently amended) The system of claim 7, wherein said feedback loop includes ~~incudes~~:

a phase detector that generates an error signal in response to the phase difference between said reference signal and said loop feedback signal;

a charge pump that provides drive currents in response to said error signal; and

a loop filter that generates said control voltage in response to said drive currents.

21. (new) An inverter system configured to lock to a reference signal, comprising:

inverters that are coupled together to form a ring and are each configured to steer an inverter current between inverter loads to provide an inverter output signal to an adjoining one of said inverters wherein the amplitude of said inverter current is a function of a control voltage and said loads have time constants that are functions of a command signal;

a feedback loop that generates said control voltage in response to the phase difference between said reference signal and an inverter output signal of any selected one of said inverters; and

a controller that alters said command signal and, hence, said time constants when said control voltage exits a predetermined control-voltage range.

22. (new) The system of claim 21, wherein each of said inverters includes:

a voltage-to-current converter that provides said inverter current and alters the amplitude of said inverter current in response to said control voltage; and

a differential pair of transistors that steers said inverter current between said inverter loads.

23. (new) The system of claim 22, wherein each of said inverters includes:

resistors;

capacitors; and

switches that, in response to said command signal, couple together selected ones of said resistors and capacitors to form said inverter loads with selected ones of said time constants.

24. (new) The system of claim 21, wherein said controller includes a comparator coupled to sense when said control voltage exits said predetermined control-voltage range.

25. (new) The system of claim 21, wherein said feedback loop includes:

a phase detector that generates an error signal in response to a phase difference between said reference signal and said inverter output signal;

a charge pump that provides drive currents in response to said error signal;

and

a loop filter that generates said control voltage in response to said drive currents.

26. (new) The system of claim 25, wherein said feedback loop further includes a frequency divider inserted to couple said inverter output signal to said phase detector.

27. (new) An inverter system configured to lock to a reference signal, comprising:

inverters that are coupled together to form a ring and are each configured to steer an inverter current between inverter loads to provide an inverter output signal to an adjoining one of said inverters wherein the amplitude of said inverter current is a function of a control voltage and a command signal;

a feedback loop that generates said control voltage in response to the phase difference between said reference signal and an inverter output signal of any selected one of said inverters; and

a controller that alters said command signal when said control voltage exits a predetermined control-voltage range.

28. (new) The system of claim 27, wherein each of said inverters includes:

capacitors coupled to form said inverter loads;

a voltage-to-current converter that provides said inverter current and alters the amplitude of said inverter current in response to said control voltage; and

a differential pair of transistors that steers said inverter current between said inverter loads.

29. (new) The system of claim 28, wherein each of said inverters includes:

current sources; and

switches that, in response to said command signal, couple selected ones of said current sources in parallel with said converter to alter said inverter current and, hence, the charging times of said capacitors.

30. (new) The system of claim 27, wherein said controller includes a comparator coupled to sense when said control voltage exits said predetermined control-voltage range.

31. (new) The system of claim 27, wherein said feedback loop includes:

a phase detector that generates an error signal in response to a phase difference between said reference signal and said inverter output signal;

a charge pump that provides drive currents in response to said error signal; and

a loop filter that generates said control voltage in response to said drive currents.

32. (new) The system of claim 31, wherein said feedback loop further includes a frequency divider inserted to couple said inverter output signal to said phase detector.

33. (new) An inverter system configured to lock to a reference signal, comprising:

ring switches;

inverters that are arranged with said ring switches to form a ring and are each configured to steer an inverter current between inverter loads to provide an inverter output signal to an adjoining one of said inverters wherein the amplitude of said inverter current is a function of a control voltage;

a feedback loop that generates said control voltage in response to the phase difference between said reference signal and an inverter output signal of any selected one of said inverters; and

a controller that commands said ring switches to thereby alter the number of said inverters in said ring when said control voltage exits a predetermined control-voltage range.

34. (new) The system of claim 33, wherein each of said inverters includes:

a voltage-to-current converter that provides said inverter current and alters the amplitude of said inverter current in response to said control voltage; and

a differential pair of transistors that steers said inverter current between said inverter loads.

35. (new) The system of claim 33, wherein said controller includes a comparator coupled to sense when said control voltage exits said predetermined control-voltage range.

36. (new) The system of claim 33, wherein said feedback loop further includes a frequency divider inserted to couple said inverter output signal to said phase detector.